REMARKS

Introduction

This Reply is in response to the Office Action of October 6, 2005. Reconsideration of this application in view of the following remarks is respectfully requested.

Claims 20-28

Claims 20-28 were withdrawn from consideration and are hereby canceled.

Claims 4, 5, 7, 8, 10-13, and 15-19

In the Office Action, claims 4, 5, 7, 8, 10-13, and 15-19 were indicated to contain allowable subject matter. Applicants reserve the right to pursue these claims during subsequent prosecution should the present Reply not be considered to place this patent application in condition for allowance.

The Rejection of Claims 1-3, 6, 9, and 14

In the Office Action, claims 1-3, 6, 9, and 14 were rejected under 35 U.S.C. §103(a) as being unpatentable over Marr. These rejections are respectfully traversed.

Claim 1 is directed to integrated circuit antifuse circuitry. The antifuse circuitry of claim 1 includes a metal-

insulator-semiconductor antifuse transistor. The antifuse circuitry also includes circuitry that applies voltages to the antifuse transistor to program the antifuse transistor.

In the Office Action, it was suggested that the transistor 1700 of FIG. 17 in Marr was the same as the antifuse transistor of claim 1. Applicants disagree.

Transistor 1700 of Marr is not an antifuse transistor. Transistor 1700 is a p-channel transistor that is used in read circuit 1011 of FIG. 10. Marr discloses antifuses in FIGS. 1, 1A, 1B, 2, 2A, and 2B, but Marr's antifuses are not formed from transistors.

Applicants explain their antifuse transistor in their specification. For example, at page 2, line 30, to page 3, line 29, applicants explain that their antifuse transistor has a gate insulator formed from an oxide such as silicon oxide. The state of the gate oxide determines the state of the antifuse transistor.

Applicants also explain how the antifuse transistor has a source, a drain, a gate, and a substrate that form a substrate-source p-n junction and a drain-substrate p-n junction. The gate oxide is broken down using localized hot carriers produced by reverse-biasing the drain-substrate junction while forward-basing the substrate-source junction.

The structure of applicants' antifuse transistor is set forth in claim 1. In particular, claim 1 is directed to an antifuse transistor having a source-substrate p-n junction and a drain-substrate p-n junction.

Marr uses a different antifuse structure. The structures that make up Marr's antifuses are shown in cross-sectional diagrams in FIGS. 1, 1A, 1B, 2, 2A, and 2B. The structure of FIG. 1 is illustrative. This structure is described on page 3, paragraphs [0051] and [0052] in Marr. As shown in FIG. 1, antifuse 150 has an n-type well 110 formed on a p-type substrate 112. N+ source diffusion region 114 and n+ drain diffusion region 116 are formed in n-type well 110.

Gate electrode 120 is connected to a first terminal 125. A second terminal 126 is connected to the source and drain diffusion regions 114 and 116. Antifuse 150 is programmed by applying a voltage of about 15 volts across the first and second terminals to rupture the gate dielectric 122.

Antifuse 150 is different than the antifuse transistor defined in applicants' claims. In particular, claim 1 specifies that applicants' antifuse transistor must have a drain-substrate p-n junction and a substrate-source p-n junction. Marr's antifuse 150 has neither of these junctions, because the n+ source diffusion region 114 and n+ drain diffusion region 116 are formed in n-well 110. Because well 110 has the same doping

type as the source and drain diffusions, there is no drain-substrate p-n junction and no substrate-source p-n junction in antifuse 150.

In rejecting claim 1, the Office Action suggested that transistor 1700 of FIG. 17 was an antifuse transistor.

Transistor 1700 is described at page 10, paragraphs [0101], [0102], [0103], and [0104] of Marr.

Paragraph [0101] of Marr explains how the read circuit 1011 of FIG. 10 has p-channel transistors 1050 and 1052 that are used instead of n-channel transistors because of their favorable noise margin properties. Although advantageous because they provide a good noise margin, the use of p-channel transistors 1050 and 1052 causes problems. In particular, when Marr's bus line 1020 is at an elevated voltage during antifuse programming, the p-channel transistors provide an undesirable path for current. Marr explains that transistor 1700 of FIG. 17 is a depiction of a p-channel transistor such as transistors 1050 and 1052 in the read circuit 1011 of FIG. 10. As shown in FIG. 10, the components of read circuit 1011 such as transistors 1050 and 1052 are distinct from antifuse 1016 and are used to read the state of antifuse 1016 after antifuse 1016 has been programmed by circuitry 1010.

The potential for undesirable current flow through the p-channel transistor 1700 is described in paragraphs [0102] and

[0103]. In paragraph [0104], Marr explains how logic circuit 1012 of FIG. 10 is used to limit this current.

As this discussion makes clear, the transistor 1700 of FIG. 17 is a p-channel read circuit transistor, not an antifuse transistor. Nothing in Marr's description of transistor 1700 or anything else in Marr shows or suggests an antifuse transistor. Claim 1, which is limited to an arrangement that contains an antifuse transistor, is therefore patentable over Marr. Claims 2-19 depend from claim 1 and are patentable because claim 1 is patentable.

Conclusion

The foregoing demonstrates that claims 1-19 are patentable. This application is therefore in condition for allowance. Reconsideration and allowance of the application are respectfully requested.

Respectfully submitted,

G. Victor Treyz 11/8/05

G. Victor Treyz
Reg. No. 36,294
Attorney for Applicants
Customer No. 45851